



Department of Electrical Engineering  
Indian Institute of Technology, Delhi  
Hauz Khas, New Delhi 110016

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Date: **October 5, 2021**

NIQ no. IITD/EE/200/2020/ATB/0002

Sealed/online/e-mail quotations are invited for fabrication of a custom integrated circuit on a  $0.18\ \mu\text{m}$  CMOS process. The required specifications are given below.

**Required Specifications for fabrication of a custom integrated circuit on a  $0.18\ \mu\text{m}$  CMOS process**

1. A custom design should be fabricated on a TSMC  $0.18\ \mu\text{m}$  process CIS process.
2. The total area of the integrated circuit is  $3000\ \mu\text{m} \times 6000\ \mu\text{m}$ , including the die-seal ring.
3. A total of at least 20 parts are required. The parts should be diced from the wafer.

**Dr. M. Sarkar**  
(Chairman, purchase committee)

## Terms and Conditions

1. The quote should reach the following address on or before **19.10.2021, 5 PM**.  
Dr. M. Sarkar  
Electrical Engineering Department  
Block II, Room 333  
IIT Delhi, Hauz Khas  
New Delhi, 110016
2. Please quote prices for FOB New Delhi, inclusive of all taxes and duties.
3. Quote should be in Indian Rupees for agents of Indian manufacturers, or in foreign currency, for agents of foreign manufacturers, and needs to be valid for at least three months.
4. Please specify all of your terms and conditions clearly, including delivery period.
5. Mode of payment for purchases in foreign currency are through irrevocable letter of credit, or through wire transfer on delivery. Only bank charges within India are payable by IIT Delhi, all bank charges outside India are the responsibility of the seller. For purchases in INR, payment is on delivery.
6. The Institute reserves the right to accept or reject any or all quotations without assigning any reasons thereof.

**Dr. M. Sarkar**  
(Chairman, purchase committee)