Department of Electrical Engineering
Indian Institute of Technology, Delhi
Hauz Khas, New Delhi 110016

NIQ no. IITD/EE/FITT-ARDE/FAB/001 Due Date: **08.05.2019, 5 PM**

Notice inviting quotations for fabrication of a custom integrated circuit on a 0.18 μm CMOS process

Sealed/online/e-mail quotations are invited for fabrication of a custom integrated circuit on a 0.18 μm CMOS process. The required specifications are given below.

Required Specifications for fabrication of a custom integrated circuit on a 0.18μm CMOS process

1. A custom design should be fabricated on a UMC 0.18μm process.
2. The total area of the integrated circuit is 6 mm x 5 mm, including the die-seal ring.
3. A total of at least 20 parts are required. The parts should be diced from the wafer.
4. The dies also needs to be packaged in a open cavity.

Dr. M. Sarkar
(Chairman, purchase committee)

Terms and Conditions

1. The quote should reach the following address on or before **08.05.2019, 5 PM**.

   Dr. M. Sarkar
   Electrical Engineering Department
   Block II, Room 333
   IIT Delhi, Hauz Khas
   New Delhi, 110016

2. Please quote prices for FOB New Delhi, inclusive of all taxes and duties.

3. Quote should be in Indian Rupees for agents of Indian manufacturers, or in foreign currency, for agents of foreign manufacturers, and needs to be valid for at least three months.

4. Please specify all of your terms and conditions clearly, including delivery period.

5. Mode of payment for purchases in foreign currency are through irrevocable letter of credit, or through wire transfer on delivery. Only bank charges within India are payable by IIT Delhi, all bank charges outside India are the responsibility of the seller. For purchases in INR, payment is on delivery.

6. The Institute reserves the right to accept or reject any or all quotations without assigning any reasons thereof.

Dr. M. Sarkar
(Chairman, purchase committee)